Schedule of Interviews for Ph.D Admissions

in Computer Science and Engineering (CSE) and Electronics and Communication Engineering (ECE) under Visveswaraya Ph.D scheme

Department	Date	Reporting Time	Serial number of eligible candidates list
Computer Science and Engineering (CSE)	10th February 2016	9.30am	CS 1 to CS 15
		1.30pm	CS 16 to CS 35
	11th February 2016	9.30am	CS 36 to CS 50
		1.30pm	CS 51 to CS 70
	12th February 2016	9.30am	CS 71 to CS 85
		1.30pm	CS 86 to CS 106
Venue for CSE: Office of Dean, Faculty of Engineering, Main Building UCE OU			
Electronics and Communication Engineering (ECE)	10th February 2016	9.30am	EC 1 to EC 15
		1.30pm	EC 16 to EC 35
	11th February 2016	9.30am	EC 36 to EC 50
		1.30pm	EC 51 to EC 70
	12th February 2016	9.30am	EC 71 to EC 85
		1.30pm	EC 86 to EC 108
Venue for ECE: Principal's Committee Room, Main Building UCE OU			

Note: Instructions to the candidates

1. Please check your serial number in the eligible candidate's list available in the website
2. All the candidates are instructed to attend the interview along with
   a) All relevant Original certificates
   b) Five copies of your Research proposal (Synopsis)
   c) ME/M.Tech thesis
   d) Research publications
3. No TA/DA will be paid for attending the interview